**Remarks**

The Examiner rejects claims 1- 5 and 17- 21 under 35 USC 103(a) as being unpatentable over Huscroft et al. (US 5,568,486), hereinafter referred to as Huscroft in view of Giorgetta et al. (US 7,053,292), hereinafter referred to as Giorgetta, and Akaike et al. (US 7,139,286) hereinafter referred to as Akaike.

In response, Applicants have amended claim 1 to recite:

A method of decoupling a time-multiplexed data stream of overhead bytes from a time-multiplexed stream of data having a variable data rate, said time-multiplexed stream of data consisting of overhead bytes and data bytes for a given path, said method comprising:

a) finding a minimum possible overhead spacing between any two consecutive unaligned floating overhead bytes in said stream of data;
b) determining a minimum interface rate by dividing said variable data rate of said stream of data by said minimum overhead spacing; and
c) interfacing between said time-multiplexed data stream of overhead bytes and said stream of data based on said minimum interface rate such that an operation of extracting overhead bytes from the stream of data is performed at a frequency that allows the overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data.

Support for the claim amendments is found in paragraphs [0034], [0053], and [0078] of the application as originally filed.

Amended claim 1 recites the features of finding a minimum possible overhead spacing between any two consecutive unaligned floating overhead bytes in the stream of data, and determining a minimum interface rate by dividing the variable data rate of the stream of data by the minimum overhead spacing between any two consecutive overhead bytes. According to the invention as recited in claim 1, interfacing between the time-multiplexed data stream of overhead bytes and the stream of data is based on the minimum interface rate such that an operation of extracting overhead bytes from the stream of data is performed at a frequency

that allows the overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data.

Huscroft discloses a method and system for extracting/inserting POH bytes assuming the presence of only nine POH bytes per 125 :s frame. However, during positive and negative pointer adjustments the number of POH bytes fluctuates above and below nine. The invention as recited in amended claim 1 is not limited to a certain number of POH bytes per frame, as the invention finds the minimum spacing between **any** two consecutive overhead bytes in order to determine a minimum interface rate. The Examiner acknowledges that Huscroft does not teach finding a minimum interface rate. Huscroft definitely fails to disclose interfacing at a frequency that allows overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data. Applicants submit that Huscroft does not teach any of method steps a, b, and c of amended claim 1.

Giorgetta is not concerned with unaligned floating data bytes, nor with finding a minimum interface rate based upon the minimum spacing between any two such consecutive overhead bytes. Furthermore, Giorgetta does not describe interfacing at a frequency that allows overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data. Applicants submit that Giorgetta adds nothing to Huscroft in light the amendments effected in claim 1.

The Examiner considers that Akaike discloses an insertion/extraction mechanism that takes into consideration floating overhead bytes and variable data rate. The differences between the present invention as recited in currently amended claim 1, and Akaike are as follows:

Akaike's interface clock is a constant clock rate that is set to 19.44 MHZ by dividing the line transmission rate (622 MHZ) by 32 (col 7, lines 9-12; col 8, lines 52-55; col 10, lines 50-53 etc.). By contrast, the minimum interface rate of the present invention is obtained by dividing the transmission rate by the minimum spacing between any two consecutive overhead bytes. The minimum spacing between any two consecutive overhead bytes is not a constant spacing because the overhead bytes are unaligned floating overhead bytes.

Additionally, the data rate of Akaike is not a variable data rate as recited in claim 1. The Examiner considers that column 3 lines 35-45 of Akaike disclose a variable data by stating "the POH data is not placed at a fixed location". Applicants respectfully disagree, because Akaike does not disclose that the data rate is a variable data rate, nor does it take this feature into consideration in the design of the system disclosed. In contrast, Akaike discloses a constant data rate e.g. 622MHZ and a constant clock e.g.19.44 MHZ (see col 7, lines 9-12; col 8, lines 52-55; col 10, lines 50-53 etc.).

Moreover, currently amended claim 1 recites interfacing based on the minimum interface rate such that an extraction operation is performed at a frequency that allows the overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data. By allowing the overhead to be extracted just before the next overhead byte arrives, the need to have more on chip buffering is eliminated. As provided in paragraphs [0037] and [0097] of the originally filed application, the invention minimizes the amount of data storage and enables a relatively low frequency of operation which reduces the circuit area, and minimizes power dissipation and noise.

In contrast, Akaike's clock (19.44 MHz), which corresponds to the bus clock of the present invention (see paragraphs [0069] and [0083] of the originally filed application), is a very fast clock for overhead insertion/extraction. This fast clock requires additional on chip buffering (col 12, lines 22-35), imposes circuit board routing restrictions, and consumes significant power relative to the slow clock used in the invention (see paragraph [0097] of the application as originally filed).

Accordingly, Akaike does not disclose any of steps a, b, and c of amended claim 1.

The Examiner relied on Akaike to show that the combination of Huscroft and Giorgetta renders claim 1 obvious. However, Akaike does not provide that which Huscroft and Giorgetta lack, and the combination of Akaike with Huscroft and Giorgetta still fails to disclose each and every element of claim 1. As none of the three steps is taught or suggested, clearly the combination of all three steps as in claim 1 cannot be taught or suggested by the cited references taken either alone or in combination.

Independent claim 17 includes all the features of claim 1, and Applicants re-iterate the same arguments in support of its patentability.

Claims 7-11, 13, and 15 have been rejected under 35 USC 103(a) as being unpatentable over Huscroft in view of Giorgetta and Akaike, and in further view of Venkataraman.

Claim 7 has been amended similar to claim 1. Applicants submit that the combination of Huscroft, Giorgetta, Akaike, and Venkataraman still fails to teach each and every element of claim 7. Venkataraman does not disclose finding a minimum interface rate based upon the minimum spacing between any two consecutive overhead bytes, nor does it teach interfacing at a frequency that allows overhead bytes to be extracted from the stream of data just before the next overhead byte for the given data path arrives in the stream of data. The same applies to Huscroft, Giorgetta, and Akaike as discussed earlier in the response. Accordingly, none of the references cited in the Official Action, whether taken alone or in combination, discloses or suggests each and every element of claim 7.

New independent claims 23 and 24 have been introduced which are similar in scope to claims 1 and 17, but recite the operation of inserting overhead bytes into the stream of data instead of extracting overhead bytes therefrom. As discussed above, the new features of claims 23 and 24 are fully supported by the application as originally filed at paragraphs [0034], [0053], and [0078].

Accordingly, each of the independent claims (1, 7, 17, 23, and 24) now being submitted has been amended to recite at least three features which are not disclosed or suggested in any of the prior art references cited in the Official Action. As none of the three features is taught or suggested, clearly the combination of all three features as in independent claims 1, 7, 17, 23, and 24, cannot be taught or suggested by the cited references taken either alone or in combination. Applicants respectfully submit each of the independent claims now being submitted is believed to comply with 35 USC 103(a).

Claims 2-6, 8-16, and 18-22 are believed to be allowable in view of their direct or indirect dependencies on claims 1, 7, 17, 23, and 24.

New claims 25 to 29 have been introduced, which recite that the frequency of operation is determined by the minimum interface rate and the cross clock domain signaling latency, as provided at paragraph [0092] of the application as originally filed.

Accordingly, it is respectfully submitted that the amended claims comply with 35 USC 103(a) and withdrawal of the rejections of the claims on that basis is respectfully requested.

It is respectfully submitted that the present application is now in condition for allowance and the Applicant looks forward to receiving an indication of patentability.

**The Commissioner is hereby authorized to debit $1,480.00 from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP, representing the fees for a Request for Continued Examination (RCE), five extra claims, and two extra independent claims.**

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

**MLAZGAR, Kevin et al.**

By: /Curtis B. Behmann/

**Curtis B. Behmann**
**Reg. No. 52,523**
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1100
Ottawa, ON K1P 1J9
CANADA
Tel: (613) 237-5160
Fax: (613) 787-3558
E-mail: ipinfo@blgcanada.com

CBB/IT/cf